REMARKS

Claims 1-19 are pending in the present application. Claims 1-4 have been amended. Claims 5-19 have been presented herewith.

Claim Rejections-35 U.S.C. 103

Claims 1-4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Beigel et al. reference (U.S. Patent No. 5,637,901). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The protection diode of claim 1 includes in combination a silicon substrate; a second conductive type impurity region; a first conductive type impurity region "on the surface of the silicon substrate so as to surround the second conductive type impurity region, the first and second conductive type impurity regions being separated from each other by a separation area having a predetermined width, the separation area including an entirety of the area between the first and second conductive type impurity regions"; an interlayer dielectric layer; a first metal interconnect layer "formed over an entirety of the second conductive type impurity region and the separation area through the interlayer dielectric layer and electrically connected to the second conductive type impurity region through a first connecting hole formed in the interlayer dielectric layer"; and a second metal interconnect layer. Applicants respectfully submit that the prior art relied upon does not make obvious these features.

The separation area of claim 1 includes an entirety of the area between the first and second conductive type impurity regions, and the first metal interconnect layer is featured as formed over an entirety of the second conductive type impurity region and the separation area. The Examiner has interpreted base region 32 in Fig. 3 of the Beigel et al. reference as the separation region of claim 1. However, base region 32 in Fig. 3 of the Beigel et al. reference does not include the entirety of the area between first and second conductive type regions as featured in claim 1, and thus can not be interpreted as the separation area of claim 1. Moreover, metallization 44 in Fig. 3 of the Beigel et al. reference is not formed over an entirety of a second conductive type impurity region and a separation area that includes an entirety of the area between first and second conductive type impurity regions, as would be necessary to meet the features of claim 1. Applicants therefore respectfully submit that the protection diode of claim 1 would not have been obvious in view of the Beigel et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1 and 2, is improper for at least these reasons.

The protection diode of claim 3 includes in combination a silicon substrate; a second conductive type impurity region; a first conductive type impurity region "formed on the surface of the silicon substrate so as to surround the second conductive type impurity region and being a predetermined width of a separation area apart from the second conductive type impurity region"; an insulating film "formed on almost an entirety of the separation area of the silicon substrate"; an electrode layer "formed on

the insulating film"; an interlayer dielectric layer "formed so as to cover the surface of the silicon substrate on which the first and second conductive type impurity regions and the electrode layer are formed"; a first metal interconnect layer; and a second metal interconnect layer.

Applicants respectfully submit that the Beigel et al. reference as relied upon by the Examiner does not include an insulating film, in addition to an interlayer dielectric layer as featured in claim 3. The Beigel et al. reference also does not include an electrode layer formed on an insulating film as featured in claim 3. Applicants therefore respectfully submit that the protection diode of claim 3 would not have been obvious in view of the Beigel et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 3 and 4, is improper for at least these reasons.

Claims 5-19

Applicants respectfully submit that claims 5-12 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner, at least by virtue of dependency on respective claims 1 and 2, and by further reason of the features therein.

The protection diode of claim 13 includes in combination a semiconductor substrate; a first impurity region; a separation area "of the semiconductor substrate surrounding the first impurity region"; a second impurity region "of the first conductivity

type, the second impurity region surrounding the separation area"; an insulating layer; an electrode layer "formed on the insulating layer, the electrode layer substantially covering an entire area of the separation area"; a first conductive pattern; and a second conductive pattern.

The Examiner has interpreted base region 32 in Fig. 3 of the Beigel et al. reference as the separation area of the claims. However, the Beigel et al. reference as relied upon by the Examiner does not include a separation area that is the same conductivity type of the semiconductor substrate, and does not include an electrode layer substantially covering an entire area of the separation area, as would be necessary to meet the features of claim 13. Applicants therefore respectfully submit that claims 13-19 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

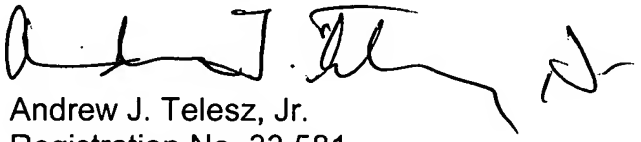
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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